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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,249	07/18/2003	Manjul Bhushan	YOR920030032US1	2874

7590 10/03/2005

Ryan, Mason & Lewis, LLP
Suite 205
1300 Post Road
Fairfield, CT 06824

EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,249	BHUSHAN ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/18/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/02/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to application 10/623,249 filed on 07/18/2003, claims 1-31 are pending.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract contains more then 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim 30 is objected to because of the following informalities: the preamble is unclear. New preamble is suggested " A apparatus for determining characteristics of metal oxide semiconductor (MOS) device including at least one circuit comprising:" As claim 1, line 24, remove "," after determining. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. The term "approximately equal" in claims 1, 3, 19, 30 and 31 is a relative term which renders the claim indefinite. The term "approximately equal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For examining purpose, Examiner interprets the term "approximately equal" as same as "substantially or nearly equal".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1–19, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (US 6,683,503) in view of Hara et al. (US 5,446,418).

9. **With respect to claims 1–19, 30 and 31**, Mizuno discloses semiconductor circuit of ring oscillator for determining characteristics of metal oxide semiconductor (MOS) devices (col. 1, ll. 9-13), which is providing a plurality of ring oscillators (figure 1,

OSC 1, OSC 2, and through OSCn), the plurality of ring oscillators have a same distance of one another (as figure 1, col. 4, ll. 25-40, -- the distance between the node. 101 and 102 are equal to 1 --); each ring oscillator comprising a plurality of coupled stages (as figure at least suggest at 110 stage coupled to stage 111 and through to 11m stages), wherein

each of the plurality of coupled stages for a first given ring oscillator comprises an inverter having at least one first MOS device having a first designed gate length (at least suggest at figure 1 and 4, see these figures description, and col. 4, ll. 50-63 – each ring oscillator has the same gate length)

each of the plurality of coupled stages for a second given ring oscillator comprises an inverter substantially identical to the inverter in couple stages of the first given ring oscillator and coupled to at least one second MOS device having a second designed gate length (at least suggest at figure 1 and 4, see these figures description, and col. 4, ll. 50-63 – each ring oscillator has the same gate length);

each of the plurality of coupled stages for a third given ring oscillator comprises an inverter substantially identical to the inverter in couple stages of the first given ring oscillator and coupled to at least one second MOS device having a third designed gate length (at least suggest at figure 1 and 4, see these figures description, and col. 4, ll. 50-63 – each ring oscillator has the same gate length)

Mizuno also discloses inverter one stage substantially identical (the same) to the inverter of coupled stage and they are also having the same channel (gate) length (figure 1 and col. 4, ll. 40-63).

Mizuno does not explicitly disclose the limitation that the second and third designed gate lengths are different and one of the second and third designed gate lengths is approximately equal to the first designed gate length. However, gate length of a transistor is well known in the art that the electrical and physical characteristics of a transistor depend on its gate length.

Hara does teach an oscillator with different gate length size for determine an input capacitance and load resistance of component (col. 3, ll. 25-63). In more specifically, figure 6 and 7 suggest the second designed gate length, such as transistor 1a, 1d and 1b, 1c equal 0.6 and 1. Figure 10 and 11 suggest the third designed gate length, such as transistor 1a, 1d and 1b, 1c equal 0.6 and 200. And figure 8 and 9 suggest the first designed gate length, such as transistor 1a, 1d and 1b, 1c equal 1 and 200. According to these gate lengths that at least suggest the second and third designed gate lengths are different and one of the second and third designed gate lengths is approximately (substantially or nearly) equal to the first designed gate length.

It would have been obvious to one of ordinary skill in the art could combine Mizuno and Hara references for employment an ring oscillator and method for characterized electrical properties of an MOS and completed device. Moreover, the electrical properties such as speed operation, power dissipate, capacitance and resistance are dependable on gate length and width of a transistor. Therefore, using different gate length in ring oscillator for generating a voltage controller with limiting current allowing measured one or more characteristics of semiconductor device such capacitance and resistance of component are related to power consumption.

10. **With respect to claim 2**, Mizuno discloses the method of claim 1, wherein the step of determining performance further comprises the steps of causing the at least one given ring oscillator to oscillate so that a delay of a coupled stage in the at least one given ring oscillator is under 30 picoseconds (at least suggest at figures 3A-3B).

11. **With respect to claim 3**, Mizuno discloses the method of claim 1, wherein the predetermined distance is approximately 1,000 microns or less (col. 2, ll. 36-42).

12. **With respect to claims 4 and 21**, Mizuno discloses the limitations of claims 1 and 19, wherein the plurality of ring oscillators are coupled together through circuitry (see figure 1).

13. **With respect to claims 5-18, 20, 22, and 25-29**, Mizuno discloses the limitations of set forth claims, (as claims 10, 20 and 22) further discloses the frequency divider couple to ring oscillator (Mizuno, figure 19) for determining a frequency and delay for each stage oscillator with substantially the same predetermine distance (Mizuno, col. 1, ll. 45-50 and ll. 61-67), but Mizuno does not explicitly disclose the different size of the gate length each MOS of ring oscillator effectively to measuring current and load capacitance per stage.

(as claims 5-10 and 25-29) Hara does discloses a ring oscillator has at least five stage coupled, each stage comprises an NMOS and PMOS are coupled in parallel from first to fifth stages. The gate lengths are increasing from the second stage to fifth stage, that will increasing limiting current and the resistance value between the drain electrodes (Hara, figures 1, for couple stages; different gate length as figures 6-11 and col. 7, ll. 20-67 and col. 8, ll. 1-23) and load capacitance per stage corresponding to the

gate size (Hara, col. 6, ll. 26-37). (as claims 11-18) Moreover, Hara is using different gate length or load capacitance and delay of ring oscillator for determining (as claim 11) physical gate length, current per unit area, gate resistance, bias length, thickness of oxide, leakage current, and power active and short circuit (Hara, col. 6, ll. 8-67 and col. 7, ll. 1-67).

It would have been obvious to one of ordinary skill in the art would combine a different gate length from the second stage to fifth stage ring oscillator of Hara's reference to oscillator in Mizuno's reference with predetermine distance between oscillators, frequency divider and delay of each stage for performed determining one or more electrical and physical characteristics for semiconductor device.

14. **With respect to claims 23 and 24,** Hara discloses wherein each of ring oscillators is coupled (connect) to independent power supply, and wherein the circuit is coupled to another independent power supply, which can be separately enable (Hara, figure 1, oscillators 1-5 and circuit 6)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M Doan
Patent Examiner
AU 2825
NMD

THUAN DO
Primary examiner.
09/29/2005